WHAT IS CLAIMED IS:

1. A tri-stable MOS latch comprising:

a first series circuit coupling first and second supply voltage terminals, with the first series circuit including a first load element coupling the first supply voltage terminal to a first node, a first biasing element coupling the first node to a second node, and a first MOS transistor, including source, drain, and gate terminals coupling the second node to the second supply voltage terminal;

a second series circuit coupling the first and second supply voltage terminals, with the second series circuit including a second load element coupling the first supply voltage terminal to a third node, a second biasing element coupling the third node to a fourth node, and a second MOS transistor, including source, drain, and gate terminals coupling the fourth node to the second supply voltage terminal;

a feedback network coupling the first node to the gate terminal of the second MOS transistor and third node to the gate terminal of the first MOS transistor;

with said first and second load elements, biasing elements, and MOS transistors fabricated utilizing MOSFET technology and with the load and biasing elements creating voltage drops to identically, within part tolerances, bias the MOS transistors in triode mode to achieve a third operating point.

2. The apparatus of claim 1 wherein:

said biasing element is a resistor.

3. The apparatus of claim 1 wherein:

said biasing element is a diode-connected transistor.

4. A tri-stable CMOS latch comprising:

a first series circuit coupling first and second supply voltage terminals, with the first series circuit including a first PMOS transistor, including source, drain, and gate terminals coupling the first supply voltage terminal to a first node, a first biasing element coupling the first node to a second node, and a first NMOS transistor, including source, drain, and gate terminals coupling the second node to the second supply voltage terminal;

a second series circuit coupling the first and second supply voltage terminals, with the second series circuit including a second PMOS transistor, including source, drain, and gate terminals coupling the first supply voltage terminal to a third node, a second biasing element coupling the third node to a fourth node, and a second NMOS transistor, including source, drain, and gate terminals coupling the fourth node to the second supply voltage terminal;

a feedback network coupling the first node to the gate terminal of the second NMOS transistor, the second node to the gate terminal of the second PMOS transistor, the third node to the gate terminal of the first NMOS transistor, and the fourth node to the gate terminal of the first PMOS transistor;

with said first and second biasing elements, and MOS transistors fabricated utilizing MOSFET technology and with the biasing elements creating voltage drops to identically, within part tolerances, bias the first and second PMOS and NMOS transistors in triode mode to achieve a third operating point.

5. The apparatus of claim 4 wherein:

said biasing element is a resistor.

6. The apparatus of claim 1 wherein:

said biasing element is a diode-connected transistor.

7. An MOS circuit comprising:

a current source;

a first clocking transistor having source, drain, and gate terminal with its source terminal coupled to the current source, where the first clocking transistor conducts when a first control signal, received at its gate terminal, is asserted;

a tristable MOS latch including:

a first series circuit coupling a first supply voltage terminal to the drain terminal of said first clocking transistor, with the first series circuit including a first load element coupling the first supply voltage terminal to a first node, a first biasing element coupling the first node to a second node, and a first MOS transistor, including source, drain, and gate terminals coupling the second node to the drain terminal of said first clocking transistor;

a second series circuit coupling a first supply voltage terminal to the drain terminal of said first clocking transistor, with the second series circuit including a second load element coupling the first supply voltage terminal to a third node, a second biasing element coupling the third node to a fourth node, and a second MOS transistor, including source, drain, and gate terminals coupling the fourth node to the drain terminal of said first clocking transistor;

a feedback network coupling the first node to the gate terminal of the second MOS transistor and third node to the gate terminal of the first MOS transistor;

with said first and second load elements, biasing elements, and MOS transistors fabricated utilizing MOSFET technology and with the load and biasing elements creating voltage drops to identically, within part tolerances, bias the MOS transistors in triode mode to achieve a third stable operating point;

a second clocking transistor having source, drain, and gate terminal with its source terminal coupled to the current source, where the second clocking transistor conducts when a second control signal, received at its gate terminal, is asserted;

an input circuit including:

first and second series circuits respectively coupling the first and third nodes to the drain terminal of the second clocking transistor, with the first series circuit including a first input transistor having source, drain, and gate terminals, the first input transistor for receiving a first input signal at its gate terminal and with the second series circuit including a second input transistor having source, drain, and gate terminals, the second input transistor for receiving a second input signal at its gate terminal;

where the tristable latch will hold any of three states previously applied to the inputs when the first control signal is a asserted and the second control signal is not asserted.

8. A method for designing a tristable latch circuit comprising the steps of:

simulating a circuit comprising a standard MOS latch having an additional biasing element, the additional biasing having an biasing characteristic, included in the cross coupling structure and with the circuit having a supplemental voltage supply, for supplying a selected value of supplemental voltage and drawing a value of a supplemental current, coupling the drains of transistors in the MOS latch;

selecting an initial biasing characteristic of the biasing element;

varying the selected value of the supplemental voltage value over a selected range;

constructing a first graph, having a first axis depicting values of the supplemental current and a second axis depicting values of the supplemental voltage, of the value of the supplemental current drawn for each selected supplemental voltage value when the biasing characteristic is equal to the initial biasing characteristic;

constructing a second graph, having a first axis depicting values of the first derivative of supplemental current as a function of the supplemental voltage value and a second axis depicting values of the supplemental voltage, of the first derivative of the supplemental current drawn as a function of the supplemental supply voltage when the biasing characteristic is equal to the initial biasing characteristic;

if the second graph of the first derivative of the supplemental current drawn as a function of the supplemental supply voltage is not a monotonic function, adjusting the biasing characteristic to an adjusted value that causes the second graph to intersect the second axis multiple times so that an MOS latch including an additional biasing element having the adjusted biasing value will have three stable operating points.

9. A method for utilizing a MOS circuit in the form of a MOS latch including an additional biasing element in the cross-coupling feedback structure, with the additional biasing element having a biasing characteristic that causes the MOS latch to have three stable operating points, said method comprising the acts of:

including the MOS circuit in a ternary logic unit that receives one of three possible input signal levels;

coupling the MOS circuit to receive the three state input signals and to latch the state of the ternary input signal accordingly.